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Systematic Control of the Nanostructure of Semiconducting-Ferroelectric Polymer Composites in Thin Film Memory Devices

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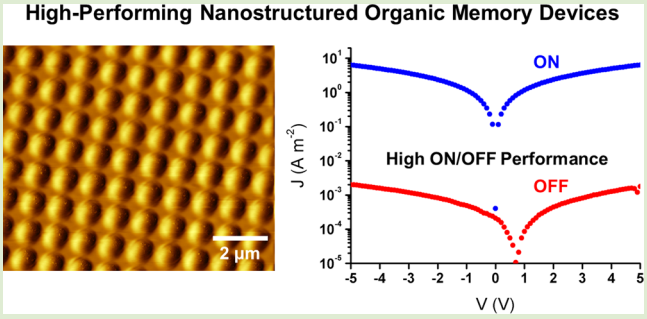
Supporting Information

ABSTRACT: In polymer-based ferroelectric diodes, films are composed of a semiconducting polymer and a ferroelectric polymer blend sandwiched between two metal electrodes. In these thin films, the ferroelectric phase serves as the memory retention medium while the semiconducting phase serves as the pathway to read-out the memory in a nondestructive manner. As such, having distinct phases for the semiconducting and ferroelectric phases have proven critical to device performance. In order to evaluate this crucial structure–property relationship, we have fabricated ordered ferroelectric devices (OFeDs) through common lithographic techniques to establish systematically the impact of nanoscale structure on the macroscopic performance. In particular, we demonstrate that there is an optimal domain size (~400 nm) for the interpenetrating networks, and we show that the ordered device, with semiconducting domains that span the entire length of the active layer film, provides a significant increase in the ON/OFF ratio relative to the blended film fabricated using standard solution blending and spin-coating techniques. This improved performance occurs due to a combination of the ordered nanostructure and the nature of the ferroelectric-semiconductor interface. As this is the first demonstration of macroscopic OFeDs, this work helps to elucidate the underlying physics of the device operation and establishes a new archetype in the design of polymer-based, nonvolatile memory devices.



Organic nonvolatile memory devices based on a blend of ferroelectric and semiconducting polymers and arranged in a sandwich geometry recently have attracted great attention due to their promise of offering a low-cost memory solution that is scalable to large areas (e.g., using crossbar array geometries).[1−6] In these composite thin films, the ferroelectric polymer is an ideal candidate for memory functionality because it is intrinsically bistable with a remnant polarization that can be switched by an applied electric field. In fact, the most commonly used polymer ferroelectric material is the random copolymer poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] due to its solution processability, large remnant polarization,[7−9] and short switching times.[9,10] To perform the electrical read-out of the memory state provided by the insulating P(VDF-TrFE), a semiconducting polymer is blended with the ferroelectric polymer resulting in a composite structure. In this bulk (or blended) heterojunction structure, free charges that are induced in the semiconductor by the poling of the ferroelectric polymer phase are passed through the electrostatically doped semiconductor in the ON state of the device.[1−6] This synergetic combination of two blended polymers has been oft-studied and relies on the storage performance of the ferroelectric phase, the read out ability of the semiconducting phase, and the ability of the two polymers to create a network for charge to be passed through the device in the ON state.

Because of the need for a continuous network in these ferroelectric diode (FeD) structures, it has been determined that the nanoscale morphology of a phase-separated blend of the two polymers is critical in device performance.[11−15] Furthermore, a recent effort utilized high-level, advanced microscopy to demonstrate that the induced charge passed during the ON state operation of these devices is present at the ferroelectric-semiconductor interface.[16] As such, both the nanostructure and the interfacial interaction of these composite thin films is of great import with respect to device performance. Many efforts have demonstrated approaches to investigate and control these properties for the optimal ferroelectric polymer diode. One very facile and promising approach is to optimize the phase-separated structure by controlling the relative ratio and domain sizes of the two polymers in this layer.[13−15] In the optimized scenarios, the semiconducting domain is continuous from the bottom electrode to the top surface electrode; this network has been determined to occur through simple spinodal decomposition of the blended polymer composite.[13] Although this strategy is very facile and useful for large-scale manufacturing purposes, it is difficult to elucidate fully the impact of nanostructure in achieving high performance in the

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functional ferroelectric diode. In order to address this issue, nanoimprint lithography-based patterning recently has been demonstrated as a method to create ordered ferroelectric polymer domains and ordered ferroelectric diodes.[17−21] In one very recent publication, nanostructured ferroelectric diodes were fabricated by using nanoimprint lithography to generate pillars of P(VDF-TrFE) that were subsequently filled with a semiconducting polymer.[21] In this careful work, improved performance of the memory device was observed at the nanoscale using advanced microscopy techniques. In addition, van Breeman et al. recently introduced a surface-directed phase separation methodology to improve device performance by optimizing the number of semiconducting polymer domains.[22] However, the macroscopic performance of these ordered ferroelectric diodes has not been reported, and the optimization of domain spacing for practical devices also has not been detailed previously.

Here, we present a series of systematically-designed active layers, composed of the ferroelectric polymer P(VDF-TrFE) and the semiconducting polymer regiorandom poly(3-hexylthiophene) (P3HT) in ordered ferroelectric device (OFeD) geometries, and we use these tailor-made designs to elucidate the impact of nanoscale morphology and interfacial interactions on the macroscopic device performance. These nanostructures are fabricated through the use of a lithographic technique in order to establish precise structure−property relationships in these composite polymeric materials. Specifically, after writing tailored nanoscale designs in the P(VDF-TrFE) template using electron-beam (e-beam) lithography, the semiconducting polymer, P3HT, was deposited into the nanoporous layer by simple solution processing. With this straightforward device fabrication methodology, we demonstrate how the nanostructure and the ferroelectric-semiconducting interface of a P(VDF-TrFE)/P3HT polymer thin film affects the memory retention performance and stability in ordered ferroelectric devices.

To demonstrate the effect of nanostructure on the memory response of the OFeDs, various square hole patterns were designed and fabricated into the P(VDF-TrFE) matrix, and the procedure of fabricating the ordered diode is shown schematically in the Supporting Information (Figure S1). Briefly, a thin film of the ferroelectric polymer P(VDF-TrFE) was spun-coat on a gold electrode, a sacrificial polymer layer, poly(methyl methacrylate) (PMMA), was cast on top of the ferroelectric layer from an orthogonal solvent (anisole), and the desired patterns were created by conventional e-beam lithography.[23−25] Reactive ion etching (RIE) was then employed to pattern the underlying P(VDF-TrFE) and remove any residual materials associated with the PMMA layer. After removal of the residual template material, the process resulted in hole patterns in the P(VDF-TrFE) thin film matrix (Figure 1a). The ratio between square pore edge length and center-to-center spacing of the pores was fixed at 1:2, while the heights of all films were set at ∼250 nm (Figure 1b). After creating the porous P(VDF-TrFE), the film was annealed at 140 °C for 2 h in order to enhance the crystallinity of the ferroelectric phase, as reported commonly in the literature.[9,26] Importantly, the patterning of the P(VDF-TrFE) domain did not affect the crystalline structure of the material relative to the unpatterned film, as shown in the Supporting Information (Figure S2). Previously, when micro- and nanoscale pillars of P(VDF-TrFE) were patterned on a substrate as the interfacial phase, an increase in the crystalline nature and the ferroelectric response of the polymer have been observed.[17] However, when the P(VDF-TrFE) is utilized as the

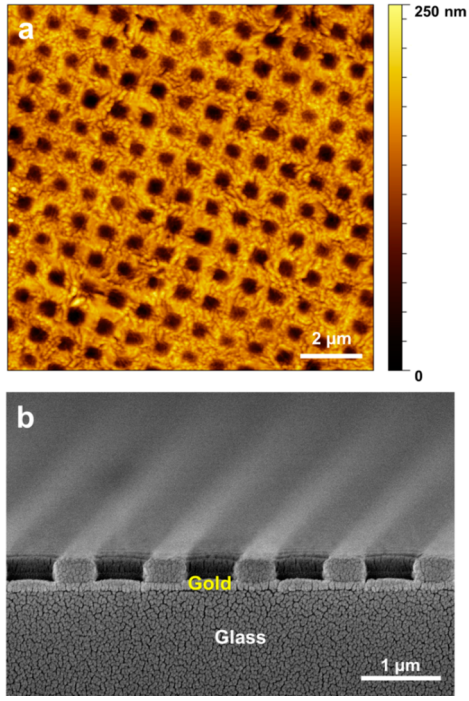

Figure 1. (a) Representative atomic force microscopy (AFM) surface topography image of a patterned P(VDF-TrFE) thin film with 500 nm pore wall edges after e-beam patterning and RIE treatment. (b) Cross-sectional SEM image of the same P(VDF-TrFE) thin film with 500 nm sized patterns on a gold-coated (100 nm) glass substrate after e-beam patterning and RIE etching.

matrix phase material, this phenomenon was not observed in our hands. On the other hand, we note that the RIE treatment did cause cross-linking within the P(VDF-TrFE) phase. This, in turn, made the nanoporous P(VDF-TrFE) template insoluble in common organic solvents. Thus, the P3HT was readily deposited on top of the nanopatterned P(VDF-TrFE) through simple spin-coating and subsequently lightly pressed into the voids using a rubbery poly(dimethylsiloxane) (PDMS) stamp. The pressure applied to the stamp was ∼0.16 bar. Finally, gold was evaporated as a top electrode to create macroscopic OFeDs with symmetric metal contacts and active areas of 4 mm.[2]

The ordered ferroelectric devices, which were patterned over macroscopic distances, were successfully realized by this strategy. Figure 2a and b show the topology and phase images of these OFeD structures, respectively, and they highlight the high degree of precise nanostructural control relative to the blended ferroelectric device active layer. For comparison, the analogous morphological and phase characterization was performed for the blended FeD structures (Figure 2c and d, respectively). In this blended active layer morphology, P3HT appears as a spherical feature in the topographical AFM image and is surrounded by a P(VDF-TrFE) matrix when the active layer is formed using standard conditions (Figure 2c).[1−6] In the blended FeD, the P3HT domains are randomly dispersed and have varying sizes, as would be expected for such a system. Also, many of the domains are continuous throughout the thin film (Figure S3), as seen previously. On the other hand, the P3HT domains of the OFeD are uniformly arranged and have almost same sizes (Figure 2a). Therefore, the well-defined structure of Figure 2a, can serve as the cornerstone of clear structure−property relationships with respect to the impact of P3HT domain size on the operation of macroscopic OFeDs

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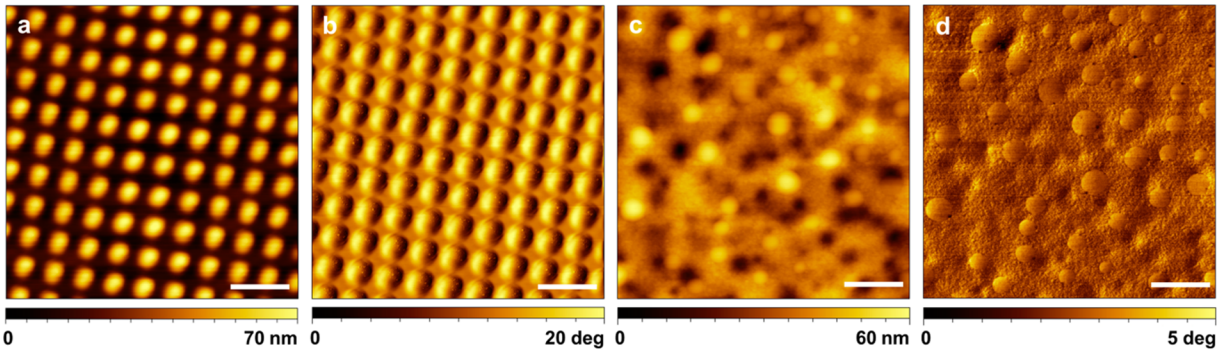

Figure 2. Comparison of the nanostructure of ordered ferroelectric diodes (a, b) and that of blended ferroelectric diodes generated by oft-used deposition conditions (c, d). (a and c) Topographic images of the patterned and the blended polymer layer, respectively. (b and d) Phase images of the ordered and blended structures, respectively. The raised (i.e., brighter) portions of (a) correspond to the P3HT domains in the ordered active layer. The structure of the ordered layer in (a) and (b) was designed to have 500 nm square patterns of P3HT embedded in the P(VDF-TrFE) matrix, and the AFM images demonstrate that this was accomplished. The blended active layer was processed according to standard conditions used in the literature (see text), and contained 10% P3HT (by weight). All in-plane dimensional scale bars are 2 μm.

due to the extremely narrow dispersity of sizes and the high degree of registry associated with these patterns.

We note that this procedure does lead to a thin skin layer of the semiconducting P3HT at the active layer-top electrode interface that varies slightly between devices and is ∼10−30 nm. This skin layer will reduce the polarizability of the ferroelectric phase and, thus, negatively impact device performance. As such, controlling and minimizing the thickness of this layer is important.

Figure 3 shows the current density−voltage response of three distinct OFeDs where the P(VDF-TrFE) was patterned with pore edge lengths of 200 (Figure 3a), 400 (Figure 3b), and 1000 nm (Figure 3c). Here, the pristine state (black trace) refers to the as-fabricated device that had undergone no electrical biasing, the ON state is referred to as the state where the entirety of the OFeD had been polarized with a −40 V bias for 5 s prior to performing the voltage sweep, and the OFF state is one in which the OFeD had been polarized with a +40 V bias for 5 s. Because gold was implemented as both the upper and the lower contacts of the device, the current density−voltage response curves are symmetric in the ON state. The work function of the gold contacts (5.1 eV) matches relatively well with the Highest Occupied Molecular Orbital (HOMO) energy level (4.9−5.0 eV) of P3HT, which is the preferred transport level of this semiconducting polymer.[27] As such, there is a nearly ohmic contact between the metal contact and the semiconducting phase, and this is the reason why the pristine curves show behavior that is similar to the ON state curves. Furthermore, this well-matched transport level design should allow for a low contact resistance for charge injection into the OFeD active layer (i.e., the OFF current density values should always be relatively high no matter the size of the pattern); however, this is clearly not the case. According to the standard ferroelectric diode operation paradigm, which relies on poor charge injection at one or both of the contacts, this device structure should not allow for memory retention characteristics. That is, without the ability to have band bending of the semiconducting P3HT to better match the work function of an initially poorly-injecting metal (e.g., silver) electrode, the device should never turn to the ON state. As such, a mechanism that includes other phenomena beyond band bending must be utilized to explain the device operation fully. Therefore, future device optimization may include both band bending (i.e., through the fabrication of devices with asymmetric metal contacts) and the phenomenon observed in these memory devices. However, we have focused these studies to elucidate the mechanism behind the rather marked ON/OFF ratio observed in the optimized active layer nanostructure (Figure 3b).

Central to this understanding is the lack of symmetry in the OFF state curves for thin films with smaller domain spacings. The OFF state curves of the devices are not symmetric around $V = 0$ V for the patterned thin films with smaller domain sizes (Figure 3a,b). That is, as the pattern size decreases, the minimum current density of the curve is shifted toward more positive voltages. This speaks directly to the idea that the P(VDF-TrFE)−P3HT interface plays a significant role in the charge transport ability of the materials because the interfacial area between the two phases increases as the patterned domain size decreases. In particular, the presence of interfacial defects would show in the OFF state current density−voltage curves through a shift in the voltage at which there was a minimum in current. This is because the applied bias would have to compensate for charges trapped at these interfaces. Previously, the utilization of reactive ion etching has proved problematic for organic electronic devices.[28,29] As such, it is possible that the patterning method itself is responsible for at least a portion of the memory retention characteristics of the OFeDs. However, across the broad range of domain spacings evaluated, it was determined that the OFeDs with the highest performance were those with domain spacings of 400 nm, in relatively good agreement with the previous results for bulk ferroelectric diode active layers composed of the same polymer blend.[13] Therefore, monitoring and elucidating the exact electrochemical nature of the states at the ferroelectric-semiconductor interface in both OFeDs and traditional ferroelectric devices could lead to significant advancements in organic memory devices.

In this work, the maximum value of the ON/OFF ratio was ∼2000 at a read-out voltage of +3 V (Figure 4a), and diodes with smaller (200 nm) or larger (1000 nm) patterns showed lower memory device performances. These characteristics in the ON/OFF ratio of the devices originate from the balance between charge induction during poling and the slowing of charge transport during read-out of the device. For instance, in the case of 200 nm patterned active layer, the ON current density of diode is 3 orders of magnitude less than the ON current density for diodes with larger nanostructural patterns (Figure 3a). This is because, as the nanoscale pattern is reduced

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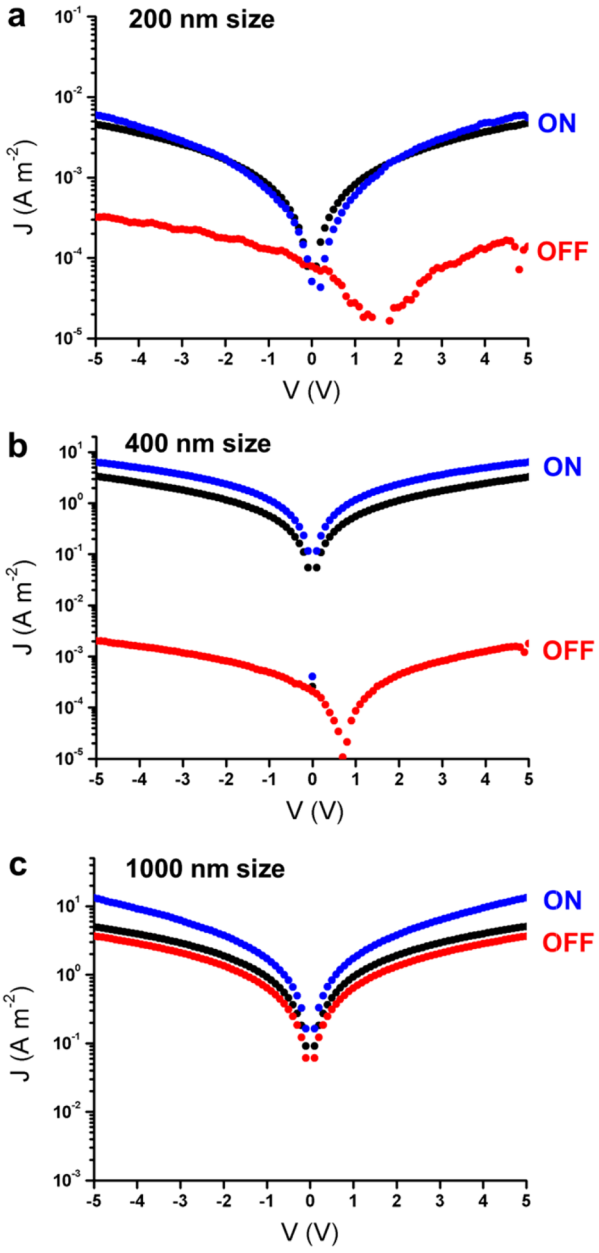

Figure 3. Representative current density−voltage characteristics of the patterned OFeD devices in the pristine (i.e., not poled; black trace), ON, and OFF states with square patterns with edge lengths of (a) 200, (b) 400, and (c) 1000 nm.

in size, there is a higher degree of P3HT−P(VDF-TrFE) interfacial contact, which increases the likelihood of the interfacial interference with the transport of charge. Previously, this has been well-explained by the idea of a counterproductive electric field that is induced upon poling;[12] however, given the results for the OFF state in the current devices, trapping due to interfacial defects should be considered as well. Due to this reduced charge transport ability, the OFeDs with smaller nanoscale patterns do not obtain ON states with high current density values even after the sufficient poling.

In contrast, the patterned devices with 1000 nm domain spacings display relatively high current density values in the ON state and the OFF state (Figure 3c). This is because the relatively small amount of interfacial interaction does not impact the charge transport ability of the semiconducting phase

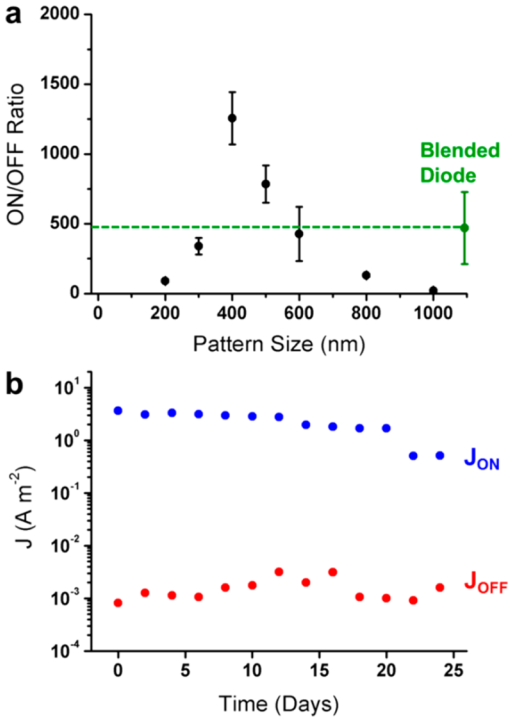

Figure 4. (a) ON/OFF ratios for the current density values of the OFeD active layers at controlled pattern sizes. All ON/OFF ratios were taken at a read-out voltage of +3 V. Each data point represents the average of six measurements, with the error bars demonstrating one standard deviation from these average values. (b) Memory durability characteristics of an OFeD with a domain size of 400 nm that were measured at a read-out voltage of V_{read} = +3 V after being programmed at −40 V or erased at +40 V.

to a great degree. However, because of the reduced interfacial area, having the device reach a low current density in the OFF state does not occur readily.

The balance between these two effects is captured well with OFeD active layers that have domain spacings of 400 nm despite the fact that band bending of the semiconducting phase does not need to occur for efficient charge injection into the device. This suggests that (1) the interface between the ferroelectric and semiconducting phase is crucial in manipulating the ON and OFF states in these OFEDs and (2) the difference between an ordered and a disordered P(VDF-TrFE) matrix is also important for the ferroelectric switching. Furthermore, it is evident that the OFeD performance can be enhanced over the traditional bulk heterojunction ferroelectric diode by this strategy, as shown in Figure 4a. The dashed green line represents the best result of a blended FeD using the same poling technique, and demonstrates readily a large decrease in ON/OFF current ratio relative to the optimized OFeD structure. In other words, by having a uniform distribution of optimal domain spacings (as opposed to an average domain spacing with a large dispersity in the blended device) that run from one electrode to another through the entire film and by taking advantage of the ferroelectric−semiconductor interface, the OFeD device structure is able to outperform the blended device structure. This improvement of device performance is also reflected in the nonvolatile memory durability (Figure 4b). Specifically, the optimized OFeD structure provides a consistent performance of ON/OFF switching up to 3 weeks. After 3 weeks, the ON state begins to decrease slightly,

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presumably due to the polarization fatigue, as observed previously.[30−37] However, the device shows a stable and reproducible behavior with an ON/OFF ratio of >100 even after 25 days. Thus, controlling the polymer nanostructure of these OFeD devices is a promising approach to achieving high durability in future nonvolatile memory devices.

In conclusion, we have controlled the nanostructure of composite polymeric materials in order to create a series of ordered ferroelectric devices through conventional lithographic techniques. These regularly patterned OFeD active layers have domain spacings as small as 100 nm and as large as 1000 nm in size for the semiconducting phase. These active layers are sandwiched between symmetric gold contacts and, despite the fact that there is nearly ohmic contact between the semiconducting phase and the metal contacts, the devices are capable of performing nonvolatile memory operations with ON/OFF current density ratios that exceed 2000. Furthermore, these high ON/OFF ratios persist for multiple weeks. Importantly, for these types of devices, we establish that the optimal domain size is one of ∼400 nm as smaller and larger domain spacings led to memory devices with smaller ON/OFF current density ratios. The physics regarding this optimum domain size is explained without relying heavily on the idea of band bending at the semiconductor−metal interface due to the fact that symmetric, ohmic gold contacts were utilized in the sandwich structure. This suggests that the ferroelectric-semiconducting interface can dominate nonvolatile memory retention. As such, the work presented within demonstrates a methodology by which to produce well-structured polymeric active layers for organic electronic memory applications and provides a new insight into the operation of these devices.

■ ASSOCIATED CONTENT

Supporting Information

Detailed experimental procedures, device fabrication scheme, GI-XRD data of the pristine and patterned P(VDF-TrFE) thin films, and cross-sectional SEM image of the blended active layer film. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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